INDIAN MARITIME UNIVERSITY
(Central University, Government of India)

May/June 2016 End Semester Examinations
B.Tech. (Marine Engineering)

Third Semester – Electronics - (UG11 T1302/ T2302)

Date : 24.06.2016 **Max. Marks: 100**
Time: 3 Hrs **Pass Marks : 50**

Part-A **(3 x10 = 30 Marks)**
Answer all the Questions

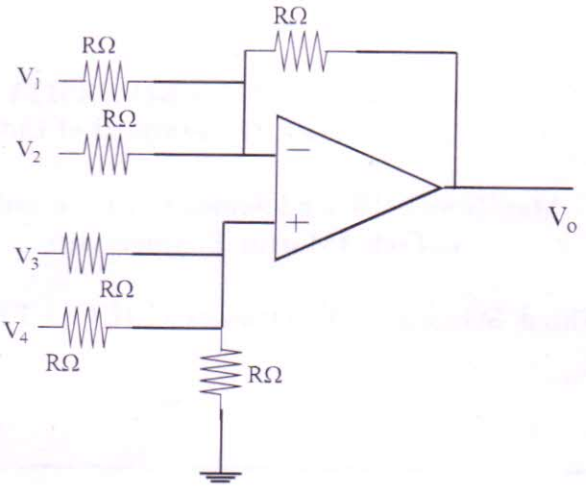
1) a) Describe the operation of T-flip-flop with timing diagram.
b) Which of the following logic is fastest
i)TTL
ii)ECL
iii)CMOS
iv)LSI
c) Define the term peak inverse voltage?
d) What is Brakhausen criteria for sustained oscillation?
e) What do you understand by combinational and sequential logic circuits?
f) What is meant by virtual ground in the op amp?
g) CMRR (Common Mode rejection Ratio) for a differential amplifier should be
(1) Zero (2) unity (3) small (4) large
h) Why emitter base junction should be in forward biased and collector based junction should be in reversed in a semiconductor junction transistor
i) Explain with block diagram principle of Digital Voltmeter using ADC
j) Where do we use FM and AM ?

Part -B **(5x14 = 70 Marks)**

Answer any five from the following eight questions

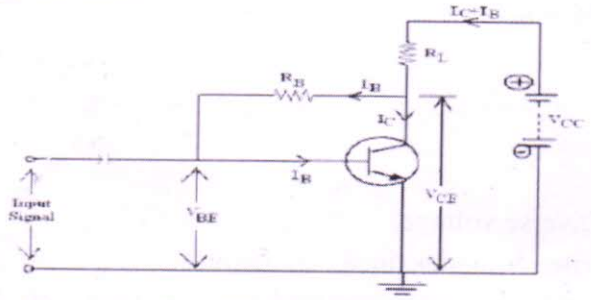
2) a) Draw and Explain the circuit of **weighted resistor** digital to analog converter (DAC). (7)
b) Realize a two input **NOR GATE** using CMOS and briefly discuss its operation. (7)

3) a) Define following terms with refers to operational amplifier (8)
a. CMRR b. Slew Rate
b) Find the output voltage V_o of the circuit shown below. (6)



4)

a) In the Figure, given bellow (7)

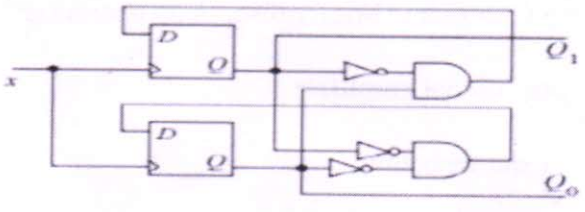


A silicon transistor with $\beta = 100$ is used as a CE amplifier with collector to base bias arrangement. The load resistance RL = 1 KΩ and VCC = 12V. Find RB so that VCE = 6V.

b) Draw and explain Wien Bridge Oscillator. (7)

5)

a) Suppose the upper D flip-flop in the below circuit were holding 1 and the lower D flip-flop held 0, while the x input were 0. Then somebody toggles the x input five times (to 1, then 0, then 1, then 0, then 1) Complete the table to show how the output values would change. (7)



x	Q_1	Q_0
0	1	0
1		
0		
1		
0		
1		

b) Simply the following Boolean function by Quine-Mc-Cluskey method $f(A,B,C,D) = \sum(2,3,6,7,8,9,13,15)$ (7)

6) a) Draw and explain diode demodulator circuit (7)

b) A broadcast transmitter radiates 5 KW , when the percentage modulation is 50 %. Calculate the total carrier power when the modulation has been reduced to 30 % (7)

7) a) For a transistor prove that collector current

$Ic = \beta I_B + (\beta+1) I_{CBO}$ (7)

Where β is the CE current gain, I_B is the base current and I_{CBO} is the collector to base leakage current.

b) In a CE transistor amplifier, the load resistance in the collector circuit is 4K ohm and Vcc = 12 V. Find the coordinates of the operating point if the zero signal base current is 20 μA and $\beta = 100$. (4)

c) How does the constructional feature of a MOSFET differ from that of a FET? (3)

8) a) Draw and explain on Push Pull Amplifier (6)

b) A transistor amplifier has a voltage gain of 50. The input resistance of the amplifier is 1 K ohm and the output resistance is 40 K ohms. The amplifier is now provided with 10 % negative voltage feed back in series with the input. Calculate the voltage gain, input and output resistance with feed back. (4)

c) Design a diode clamper circuit to clamp the positive peaks of the input signal at zero level. The frequency of the input voltage is 500 Hz.(Diode forward resistance R_f= 1 Kohm and Diode reverse resistance Rr = 200 K ohm) (4)

9) a) Draw and explain class A amplifier. (7)

b) In a CE transistor amplifier the load resistance in the collector circuit is 4K Ω and VCC = 12 V . Find the Q point of operation. If zero signal base current is 20 μA and $\beta = 100$ (7)

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